SEMICONDUCTOR DEVICES AND METHODS FOR MANUFACTURING THE SAME

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Technical Field

The present invention includes semiconductor devices having a bonding pad region and methods for manufacturing the same.

Related Art

Presently, with further miniaturization of semiconductor devices being advanced, wiring layers in semiconductor devices are formed in multiple layers. A semiconductor device is generally provided with a pad opening section that reaches the uppermost layer among the wiring layers. The exterior and the uppermost layer among the wiring layers are electrically connected through the pad opening section.

Fig. 9 schematically shows a cross-sectional view of a pad forming region of a semiconductor device. Generally, wiring layers 332 and 330 that are formed at a level below the wiring layer 340 which the pad opening section reaches are also formed in a region below the pad opening section 360. However, when the wiring layers 332 and 330 are formed in a region below the pad opening section 360, cracks 310 may be generated in interlayer insulation layers 322 and 324, when wiring bonding is carried out at the pad opening section 360.

Summary

Certain embodiments relate to a semiconductor device including a protective insulation layer, a pad opening section provided in the protective insulation layer, a wiring

layer which the pad opening section reaches, and a wiring layer provided at a level lower than the upper wiring layer. The wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

Embodiments also relate to a semiconductor device including a first wiring layer formed above a semiconductor layer through a first interlayer insulation layer, a second wiring layer that provides a pad section formed above the first wiring layer through a second interlayer insulation layer, a protective insulation layer formed above the second wiring layer and the second interlayer insulation layer, and a pad opening section provided in the protective insulation layer. An upper surface of the first interlayer insulation layer includes a first region where the protective insulation layer is formed vertically thereabove, and the first wiring layer is formed on the first region.

Embodiments also relate to a method for manufacturing a semiconductor device, the method including the steps of: (a) forming a wiring layer on an interlayer insulation layer; (b) forming a protective insulation layer on the interlayer insulation layer and the wiring layer; and (c) forming a pad opening section in the protective insulation layer, which reaches the wiring layer. The semiconductor device is formed to include a wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches. The pad opening section is formed such that the wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

Embodiments also relate to a method for manufacturing a semiconductor device, including forming a lower level wiring layer; forming an lower level interlayer dielectric layer on and adjacent to the lower level wiring layer; forming an upper level wiring layer above the lower level interlayer dielectric layer, wherein the lower level wiring layer is electrically connected to the upper level wiring layer; and forming a protective insulation layer on the upper level wiring layer. The method also includes removing a first portion of the protective insulation layer over the upper level wiring layer and over the lower level interlayer dielectric layer to form a pad opening section in the upper level wiring layer,

wherein a second portion of the protective insulation layer located vertically above the lower level wiring layer remains after removing the first portion of the protective layer; and wherein no portion of the lower level wiring layer is disposed vertically below the pad opening section.

Brief Description of the Drawings

Embodiments of the invention are described with reference to the accompanying drawings which, for illustrative purposes, are schematic and not necessarily drawn to scale.

Fig. 1 schematically shows a cross-sectional view of a semiconductor device in accordance with one embodiment of the present invention.

Fig. 2(a) shows an enlarged plan view of a region A10 of Fig. 1, and Fig. 2(b) schematically shows a cross-sectional view taken along lines A – A of Fig. 2(a).

Fig. 3 schematically shows a cross-sectional view of a semiconductor device in a modified example.

Fig. 4 schematically shows a cross-sectional view of a plug in a modified example.

Fig. 5 schematically shows in cross section a step of forming a plug in accordance with a modified example.

Fig. 6 schematically shows in cross section a step of forming a plug in accordance with a modified example.

Fig. 7 schematically shows a cross-sectional view of a section of a semiconductor device in accordance with a modified example.

Fig. 8 shows a plan view of a plane pattern of first plugs and second plugs.

Fig. 9(a) schematically shows a plan view of a semiconductor device in accordance with a conventional example, and Fig. 9(b) schematically shows a cross-sectional view taken along lines B – B of Fig. 9(a).

Fig. 10 schematically shows an illustration of problems of the semiconductor device of the conventional example.

Detailed Description

Certain embodiments of the present invention provide semiconductor devices in which generation of cracks in interlayer insulation layers below a wiring layer which a pad opening section reaches is suppressed and methods for manufacturing the same. A first semiconductor device in accordance with certain embodiments of the present invention comprises: a protective insulation layer; a pad opening section provided in the protective insulation layer; a wiring layer to which the pad opening section reaches; and a wiring layer provided at a level lower than the wiring layer which the pad opening section reaches, wherein the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

It is noted that the "wiring layer provided at a level lower than the wiring layer which the pad opening section reaches" means a wiring layer that is formed in an interlayer insulation layer provided below an interlayer insulation layer in which the wiring layer which the pad opening section reaches is formed.

In accordance with preferred embodiments, a wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view. In other words, a wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is not formed in a region below the pad opening section. Accordingly, even when an impact is inflicted on the wiring layer which the pad opening section reaches when wire bonding is conducted, the impact can be received by the interlayer insulation layer. As a result, generation of cracks in an interlayer insulation layer provided below the wiring layer which the pad opening section reaches can be suppressed.

The wiring layer which the pad opening section reaches may be composed of one layer in one embodiment, or two layers in another embodiment.

The wiring layer which the pad opening section reaches may be provided with a thickness that is greater than that of the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches.

A second semiconductor device in accordance with certain embodiments of the present invention comprises: a first wiring layer formed above a semiconductor layer through a first interlayer insulation layer; a second wiring layer that provides a pad section formed above the first wiring layer through a second interlayer insulation layer; a protective insulation layer formed above the second wiring layer and the second interlayer insulation layer; and a pad opening section provided in the protective insulation layer, wherein an upper surface of the first interlayer insulation layer includes a first region where the protective insulation layer is formed vertically there above, and wherein the first wiring layer is formed on the first region.

The upper surface of the first interlayer insulation layer may further comprise a second region where the pad opening section is formed vertically there above, and an insulation layer is mainly formed on the second region.

The first wiring layer may further comprise a plurality of wiring layers in the same layer, and the plurality of wiring layers may be formed on the first region.

A method for manufacturing a semiconductor device may comprise the steps of: (a) forming a wiring layer on an interlayer insulation layer; (b) forming a protective insulation layer on the interlayer insulation layer and the wiring layer; and (c) forming a pad opening section in the protective insulation layer, which reaches the wiring layer; wherein the semiconductor device includes a wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches; and wherein the pad opening section is formed such that the wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

Certain preferred embodiments of the present invention are described below with reference to the accompanying drawings.

Fig. 1 schematically shows a cross-sectional view of a semiconductor device. Fig. 2(a) shows an enlarged view of a region A10 of Fig. 1. Fig. 2(b) schematically shows a cross-sectional view taken along lines A – A of Fig. 2(a).

First, a plane structure of a semiconductor device 1000 is described. The semiconductor device 1000 includes, as shown in Fig. 1, an active region 100 and a pad region 200. The pad region 200 is formed along the periphery of the active region.

Next, a cross-sectional structure of the semiconductor device 1000 is described. A semiconductor element is formed on a surface of the semiconductor substrate 10 in the active region. The semiconductor element includes one or more transistors, for example, MIS and/or memory transistors. A first interlayer insulation layer 20 is formed on the semiconductor substrate 10. A first wiring layer 30 is formed on the first interlayer insulation layer 20. A second interlayer insulation layer 22 is formed on the first interlayer insulation layer 20 and the first wiring layer 30. More specifically, when the first interlayer insulation layer 20 defines a first region on its upper surface above which a protective insulation layer 50 (to be described below) is formed, the first wiring layer 30 is formed on the first region. Also, when the first interlayer insulation layer 20 defines a second region on its upper surface above which a pad opening section 60 (to be described below) is formed, the second interlayer insulation layer 22 is formed on the second region. First plugs 70 are formed in the second interlayer insulation layer 22 for electrically connecting the first wiring layer 30 and a second wiring layer 32.

The second wiring layer 32 is formed on the second interlayer insulation layer 22 and the first plugs 70. A third interlayer insulation layer 24 is formed on the second interlayer insulation layer 22 and the second wiring layer 32. More specifically, when the second interlayer insulation layer 22 defines a third region on its upper surface above which the protective insulation layer 50 (to be described below) is formed, the second wiring layer 32 is formed on the third region. Also, when the second interlayer insulation layer 22 defines a fourth region on its upper surface above which the pad opening section 60 (to be described below) is formed, the third interlayer insulation layer 24 is formed on the fourth region.

A third wiring layer 40 is formed on the third interlayer insulation layer 24. The third wiring layer 40 may preferably have a thickness that is greater than either the first wiring layer 30 or the second wiring layer 32. Second plugs 72 are formed in the third

interlayer insulation layer 24 for electrically connecting the third wiring layer 40 and the second wiring layer 32.

A protective insulation layer 50 is formed on the third interlayer insulation layer 24 and the third wiring layer 40. A pad opening section 60 is formed in the protective insulation layer 50. The pad opening section 60 reaches the upper surface of the third wiring layer 40. The pad opening section 60 has a width of, for example, 30 – 150 μm. A plane area of the pad opening section 60 is, for example, $30 \times 30\ \mu m^2$ to $150 \times 150\ \mu m^2$. For example, wire bonding is conducted in the pad opening section 60 for electrically connecting the exterior and the third wiring layer 40.

Next, certain characteristic aspects of the present embodiment are described. The first and second wiring layers 30 and 32 which are formed at a level below the third wiring layer 40 are formed outside a region of the pad opening section 60 as viewed in a plan view. In other words, the first and second wiring layers 30 and 32 are not formed below the region of the pad opening section 60. Accordingly, even when an impact is inflicted on the third wiring layer 40 when wire bonding is conducted, the impact can be received only by the interlayer insulation layers 20, 22 and 24. As a result, generation of cracks in the interlayer insulation layers 20, 22 and 24 provided below the third wiring layer 40 can be suppressed. Also, exfoliation of films at boundaries between the wiring layers and the interlayer insulation layers can be suppressed.

A method for manufacturing a semiconductor device in accordance with one embodiment of the present invention is described below with reference to Fig. 2.

First, a semiconductor element (for example, one or more MIS transistors or memory transistors) is formed on the semiconductor substrate 10. Next, a first interlayer insulation layer 20 composed of silicon oxide is formed by a known method. The first interlayer insulation layer 20 may be planarized, depending on the requirements, by a chemical-mechanical polishing method (CMP method).

Next, a first wiring layer 30 is formed on the first interlayer insulation layer 20. The first wiring layer 30 may be provided by forming a conduction layer (for example, an aluminum layer or an alloy layer including aluminum and copper) by a known method, and

patterning the conduction layer. The first wiring layer 30 is formed in a region other than the region where the pad opening section 60 is formed.

Next, a second interlayer insulation layer 22 composed of silicon oxide is formed on the first wiring layer 30 and the first interlayer insulation layer 20 by a known method. The second interlayer insulation layer 22 may be planarized depending on the requirements by a CMP method. Then, through holes 22a that reach the first wiring layer 30 are formed in the second interlayer insulation layer 22. The through hole 22a has a width of, for example, 0.2 – 0.5 μm. A plane area of the through hole 22a is, for example, $0.2 \times 0.2\ \mu m^2$ to $0.5 \times 0.5\ \mu m^2$. Then, first plugs 70 are formed in the through holes 22a. The first plugs 70 are provided by, for example, forming a layer of tungsten on the entire surface, and etching-back the tungsten layer.

Next, a second wiring layer 32 is formed on the first plugs 70 and the second interlayer insulation layer 22. The second wiring layer 32 may be provided by forming a conduction layer (for example, an aluminum layer or an alloy layer such as an alloy including aluminum and copper) by a known method, and patterning the conduction layer. The second wiring layer 32 is formed in a region other than the region where the pad opening section 60 is formed.

Next, a third interlayer insulation layer 24 composed of silicon oxide is formed on the second interlayer insulation layer 22 and the second wiring layer 32 by a known method. The third interlayer insulation layer 24 may be planarized depending on the requirements by a CMP method. Then, through holes 24a that reach the second wiring layer 32 are formed in the third interlayer insulation layer 24. The through hole 24a has a width of, for example, 0.2 – 0.5 μm. A plane area of the through hole 24a is, for example, $0.2 \times 0.2\ \mu m^2$ to $0.5 \times 0.5\ \mu m^2$. Then, second plugs 72 are formed in the through holes 24a. The second plugs 72 are provided by, for example, forming a layer of tungsten on the entire surface, and etching-back the tungsten layer.

Next, a third wiring layer 40 is formed on the third interlayer insulation layer 24 and the second plugs 72. The third wiring layer 40 may be provided by forming a conduction

layer (for example, an aluminum layer or an alloy layer such as an alloy including aluminum and copper) by a known method, and patterning the conduction layer.

Next, a protective insulation layer (for example, a silicon oxide layer) 50 is formed on the third wiring layer 40 by a known method. Then, using a lithography technique, the protective insulation layer 40 is selectively etched, to form a pad opening section 60 that reaches the third wiring layer 40. The pad opening section 60 is formed such that the first and second wiring layers 30 and 32 are disposed outside a region of the pad opening section 60 as viewed in a plan view.

Effects which may be provided by the method for manufacturing a semiconductor device in accordance with the present embodiment are described.

In accordance with the present embodiment, the first and second wiring layers 30 and 32 are formed outside a region of the pad opening section 60. Accordingly, the first and second wiring layers 30 and 32 are not formed vertically or directly below the region of the pad opening section 60, as seen in Fig. 2(b). Instead, the first and second wiring layers 30 and 32 are to the side and lower than the pad opening section 60. Another way to describe the relationship is that the first and second wiring layers 30 and 32 are formed outside of the region defined by the width (or perimeter) of the pad opening section and extending vertically downward from the pad opening section 60. As a result, stresses generated when wire bonding is conducted can be received only by the first through third interlayer insulation layers 20, 22 and 24. Therefore generation of cracks in the interlayer insulation layers 20, 22 and 24 can be suppressed. Also, separation of films at boundaries between the interlayer insulation layers and the wiring layers can be suppressed.

Examples of modifications which can be made to the present embodiment are set forth below as modified examples (1) - (7).

(1) In the embodiment described above, the third layer 40 is formed from a single layer. However, as shown in Fig. 3, a third wiring layer 140 may have a two-layer structure. More specifically, the third wiring layer 140 may have the following structure. The third wiring layer 140 includes a lower wiring layer 140a and an upper wiring layer 140b. An insulation layer 80 is provided on the lower wiring layer 140a, and a through hole 82 is

provided in the insulation layer 80. The upper wiring layer 140b is formed in a manner to fill the through hole 80, and also preferably formed to extend over at least a portion of the insulation layer 80.

It is noted that the third wiring layer 140 may also be formed from three layers or more.

(2) The second plug 72 for electrically connecting the second wiring layer 32 and the third wiring layer 40 may have the following structure. As shown in Fig. 4, a titanium film 90 and a titanium nitride film 92 may be provided between the second plug 72 and the third interlayer insulation layer 24. The thickness of the titanium film 90 may be, for example, 10 – 20 nm. The thickness of the titanium nitride film 92 may be, for example, 20 – 80 nm.

The titanium film 90, the titanium nitride film 92 and the second plug 72 may be formed as follows as an example. Methods known in the art for depositing and processing the various layers may be used. First, as shown in Fig. 5, a through hole 24a that reaches the second wiring layer 32 is formed in the second interlayer insulation layer 24. Then, the titanium film 90 and the titanium nitride film 92 are successively formed on the entire surface. Then, a tungsten layer 72a is deposited. Next, as shown in Fig. 6, the tungsten layer 72a is planarized to form the second plug 72. Then, the titanium film 90 and the titanium nitride film 92 that are formed on the second interlayer insulation layer 24 are removed. For removing the titanium film 90 and the titanium nitride film 92, methods which may be used include, for example, a method using a CMP method to polish and remove them and a method using a lithography technique to selective etch them can be used.

(3) The first plug 70 may have the same structure as that of the second plug 72 in the modified example (2).

(4) In the modified example (2), as shown in Fig. 7, the titanium film 90 and the titanium nitride film 92 may not be removed, and the titanium film 90 and the titanium nitride film 92 may be interposed between the second interlayer insulation layer 24 and the third wiring layer 40.

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(5) A reflection prevention film may be formed on the third wiring layer 40. It is noted that, when a reflection prevention film is formed, the reflection prevention film at the

pad opening section 60 may preferably be removed in order to improve the coherency between bonding structures (for example, bonding balls, bumps, etc.) and the third wiring layer 40. The reflection prevention film may be formed from, for example, a titanium nitride film. The thickness of such a titanium nitride film is, for example, 20 – 80 nm.

(6) In the embodiment described above, the wiring layer provided below the third wiring layer 40 consists of the first wiring layer and the second wiring layer, in other words, two layers. However, one wiring layer or three or more wiring layers may alternatively be provided below the third wiring layer 40.

(7) The first plugs 70 may be formed in a staggered manner, as shown in Fig. 8. Also, the second plugs 72 may be formed in a staggered manner, as shown in Fig. 8. The second plugs 72 can be formed such that they do not overlap the first plugs as viewed in a plan view.

By connecting the first wiring layer 30 and the second wiring layer 32 through a plurality of first plugs 70, as shown in Fig. 2(b) and Fig. 8, even when any of the plural first plugs 70 becomes non-conductive, the electrical connection between the first and second wiring layers can be secured by other of the first plugs 70. Also, by providing the plural plugs, the electromigration resistance can be improved. When a plurality of second plugs 72 are provided, the electrical connection between the second wiring layer 32 and the third wiring layer 40 becomes more reliable, and the electromigration resistance can be improved, in the same manner as the plurality of first plugs 70.

Also, by disposing the second plugs 72 in a manner to avoid overlapping the first plugs 70 as viewed in a plan view, the electrical resistance between the first plugs and the second plugs can be lowered.

The present invention is not limited to the embodiments described above, and many changes can be made within the scope of the subject matter of the present invention.